MPM-400G™
400G Multi-Protocol Module

MPA Multi-Protocol Analzyer
Modular Test Platform

Specifically designed to meet the test and measurement challenges of developers and early adopters of 400G ASICs, CFP8 optics, transport/switching modules, and service delivery.

Module Highlights

- 400G test module with native support for 400G CFP8 pluggable optics
- 400G Ethernet testing per IEEE 802.3bs (16 x 26.5625G/425G) with RS (544, 514) KP4 Forward Error Correction (FEC)
- Provides all the necessary features to test CFP8 modules and the 400GE data pipe
- Advanced and flexible FPGA based test module provides future proof hardware support for emerging standards
- The advanced pluggable hardware module supports can operate in parallel with other additional test modules.
- 1U MPA chassis supports up to 2x MPM-400G test modules plus additional test modules

Applications

- Comprehensive 400GE test applications for layers 1-4
- Full rate 400GE BERT, throughput and frame loss measurements
- PCS & RS-FEC layer testing with skew generation and analysis
- Service disruption time measurement
- CDAUI-16 16x25G signal integrity testing with multi-lane unframed BERT
- High speed lane clock stressing/analysis and optical power level verification

CFP8 Interface

- Native support for 400G CFP8 modules
- Supports any MSA and IEEE 802.3bs compliant CFP8 module
- Supports CDAUI-16 (16x25G) electrical interface to CFP8

PCS/RS-FEC Layer

400GE PCS/FEC Lane Numbering

- Supports lane number swapping and rotation
- Displays received lane ID, lane # and channel assignments

400GE PCS/FEC Lane Skew

Static Skew Generation

- Per lane static skew generation 0 to 4,158 bits

Skew Analysis

- Per lane skew analysis in bit time and picoseconds, 66-bit resolution up to 4,158 bit periods
- User defined alarm threshold for received skew measurement

Error Generation

FEC Uncorrectable

- Per channel A, B, or A+B
- 3.33E-3 to 1E-9 rates
- Single error insert

FEC Correctable

- Per channel A, B, or A+B
- 1E-3 to 1E-10 rates
- Single error insert
- Periodic burst
  - Burst size: 1-15 symbol errors per codeword
  - Period: Number of codewords or milliseconds; single burst

FEC Correctable Symbol

- Generates 1 symbol error per codeword
- Per FEC lane: 1 to N lanes
- 1E-3 to 1E-10 rates
- Single error insert

FEC Correctable Bit

- Generates single bit error per codeword
- Per FEC lane: 1 to N lanes
- 1E-3 to 1E-10 rates
- Single error insert

FEC Transcode

- 1E-3 to 1E-10 rates
- Single error insert

Block

- 64B/66B Block/Code single, 1E-3 to 1E-10 rates
- Single error insert

Alarm Generation

Duration: continuous

- FEC LOA
- High SER
- FEC Alignment marker loss per lane

FEC Stress Test

The advanced FEC stress test provides a one-button method to ensure R&D FEC receiver designs can correct the maximum number of errors over the entire data path.

The test simulates actual optical line errors on the outgoing line injecting 15 symbol errors in the RS FEC block using a pseudo-random 10-bit error mask and a pseudo random symbol error location that guarantees all symbol locations in the RS FEC block will be errored in roughly 1 µsec. The FEC Stress Test can be performed on FEC channel A, B, or A+B.

Error Results

Measures error counts, average and current rates

Per Channel FEC Errors

FEC A+B

- Uncorrectable codeword errors
- Correctable codeword Errors
- Correctable symbols errors
- Correctable one bit error
- Correctable zero bit error

FEC A

- Uncorrectable codeword errors
- Correctable codeword Errors
- Correctable symbols errors
- Correctable one bit error
- Correctable zero bit error

FEC B

- Uncorrectable codeword errors
- Correctable codeword Errors
- Correctable symbols errors
- Correctable one bit error
- Correctable zero bit error

Per Lane FEC Errors

- Correctable symbol error
- FEC Correctable bit error

FEC Symbol Error Analysis

- The advanced FEC symbol error analysis feature provides the number of symbol errors per codeword along with their percentage to the total correctable codewords

FEC Transcode Error

Alarm Results

Alarm Detection: Seconds

- FEC LOA
- High SER
- FEC Alignment marker loss per lane (LOAMPS)
- FEC SER

FEC Degraded SER

- Supports FEC Degraded Ser Monitoring
- FEC Degraded SER Alarm seconds
- SER Degrade Interval: 0 to 65,535 codewords
- SER Active and Deactivate Thresholds: 0 to 65,535 Symbols (range dependent on configuration)

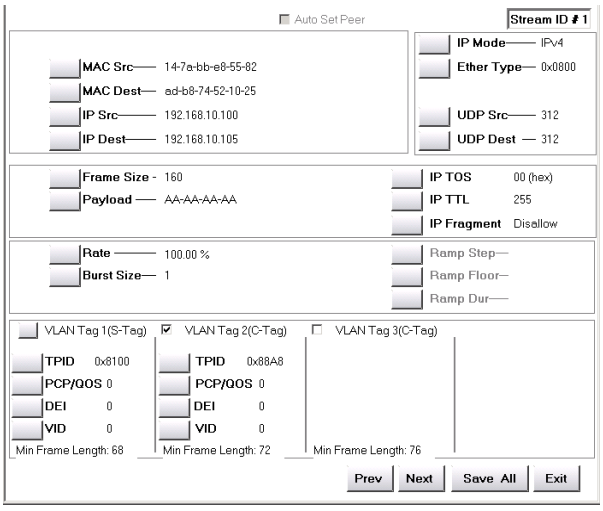
Ethernet/IP Layer

Traffic Generation/Test Stream Flow

- Test stream flow with generation and analysis capability with separate rate, addressing and traffic parameters
- Test flow is generated with a signature field in the beginning of the UDP payload area for traceability and measurement purposes
- MAC/IP/UDP formatted traffic generation
- IP Version: IPv4 or IPv6
- MAC/IP/UDP source and destination addressing
- User defined Ethernet Type, Traffic Class, Hop Limit, Flow label fields
- Frame sizes: 60 to 16,000 bytes
- Test Pattern: 2^{31}-1 normal and inverted, 32-bit user
- VLAN tags up to 4 levels with user defined TPID, PCP/QOS, DEI, VID
- MPLS tags up to 4 levels with user defined label, TC, S(bottom), TTL

Traffic Rate Generation

- Full rate generation and analysis
- Constant rate by % BW with 0.01% resolution and accuracy
- Constant rate by Mbps with 0.001Mbps resolution and accuracy
- Constant rate by average interpacket gap in bytes with approximately 1 byte accuracy
- Constant rate by average interpacket gap in ms with approximately 1 ms accuracy
- Ramp by %BW or Mbps with configurable ramp ceiling, floor, step size and step size duration
- Burst size with single burst of traffic from 1 frame to 1 second of frames at minimum interpacket gap



Configurable Preamble/SFD

Supports configurable of preamble and SFD for all port generated test stream traffic

Flow Control

- Port responds to received pause frames with option enable/disable
- Generate pause packet with 0 to 65535 quanta
- Counts transmitted and received pause packets, pause quanta and pause end packets

Error Generation

- Payload Bit (single, 1E-3 to 1E-10 rates)
- Sequence (single, 1E-2 to 1E-7 rates)
- Runt (single, 1E-2 to 1E-7 rates), configurable 60-63byte size
- FCS (single, 1E-2 to 1E-7 rates)
- IP Checksum (single, 1E-2 to 1E-7 rates)
- UDP Checksum (single, 1E-2 to 1E-7 rates)

Alarm Generation

- Remote and local fault alarms
- Auto reply to local fault option

RFC 2544 Benchmarking

- Throughput/Latency, Frame loss, Back to Back Burst
- Automated test sequence allows single or all tests to be run in sequence

Supports standardized and configurable parameters including graphical results

- Up to 8 configurable frame size test steps
- Trial duration, min/max transmit bandwidth
- Throughput acceptable loss rate, latency iterations, and resolution rate
- Back to Back burst - configurable resolution and number of repetitions

Service Disruption Time (SDT) Measurement

- Event Triggers: loss of Ethernet frame disruption, FCS error
- Event thresholds: minimum SDT time (0.1 to 1683.3ms), measurement clearing time (10.0 to 1638.3ms)
- 0.1ms resolution and accuracy
- Single or continuous measurements
- Reports SDT min, max, and average values
- Displays the last measurement plus 10 historical events, last 250 events saved in test report
- SDT accuracy is dependent on transceiver performance, particulary for LOS events

Results

Result Filtering

Results can be filtered by up to 4 VLAN tag TPIDs

Transmit and Receive Port Counts

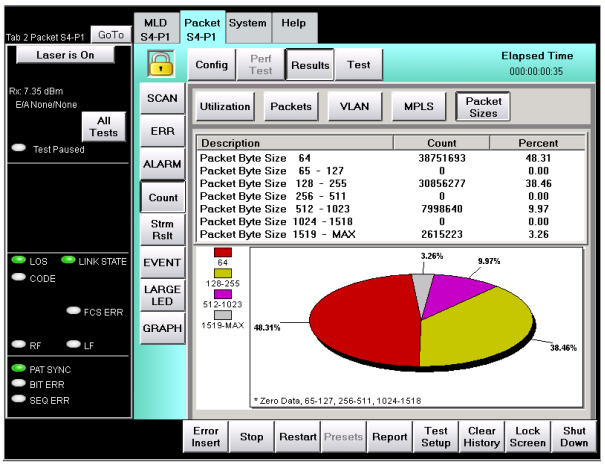
- Packets, packets/second, bytes, Mbps, % BW
- VLAN packets, MPLS packets
- IPv4 & IPv6 packets

Receive Port Counts

- TCP, UDP, IGMP, ICMP packets
- Broadcast, multicast, unicast
- Jumbo, super jumbo packets (greater than 9216 bytes)

Distribution Results

- VLAN distribution by tag level and quality of service level
- MPLS distribution by tag level and traffic class
- Packet size distribution for 64, 65-127, 128-255, 256-511, 512-1023, 1024-1518, 1519–max byte ranges with support for counts, percentage and graphing



Utilization Counts

- Total, IPv4, IPv6, VLAN, MPLS binning
- Current, min, max, and average % BW, Mbps, and packets per second statistics for generated and received traffic

Errors

Displays counts, errored seconds, current and average error rates

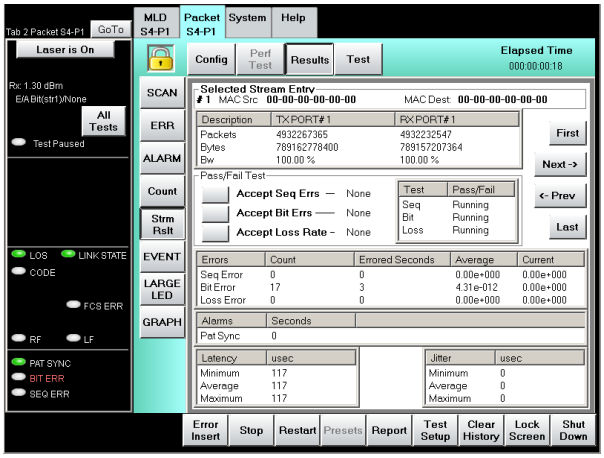
Alarms

Loss of link, local fault, remote fault

Test Stream Results

Independent set of test stream performance results

- Transmitted and received packet counts, byte counts and rate in %BW
- Test stream sequence errors, bit errors and lost frame counts in errored seconds, current and average rates
- User-defined pass/fail threshold alarm from sequence errors, bit errors and lost frames
- Latency min, max, and average measurements with 0.1µsec resolution and accuracy
- Packet jitter min, max, and average measurements with 0.1 µsec resolution and accuracy

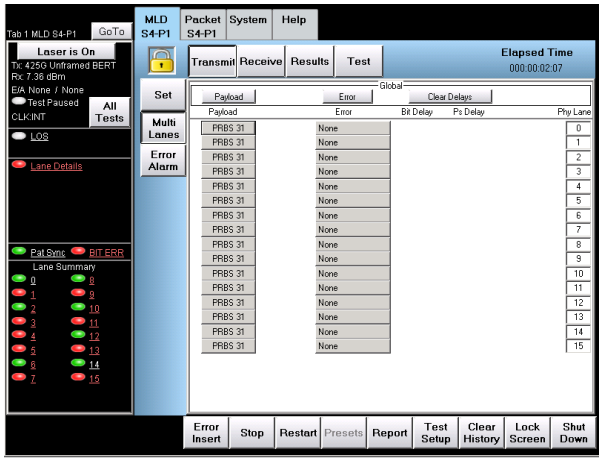


Multi-lane Unframed BERT Testing

Per lane BERT testing for transceiver and equipment characterization and acceptance testing

Test Patterns

- Modes: 16 x 26.5625G
- PRBS 2^{31}-1, 2^{23}-1 ,2^{20}-1, 2^{15}-1, 2^{11}-1, 2^{9}-1 normal or inverted
- Per lane test pattern selection, error generation and BER analysis



Clock Source

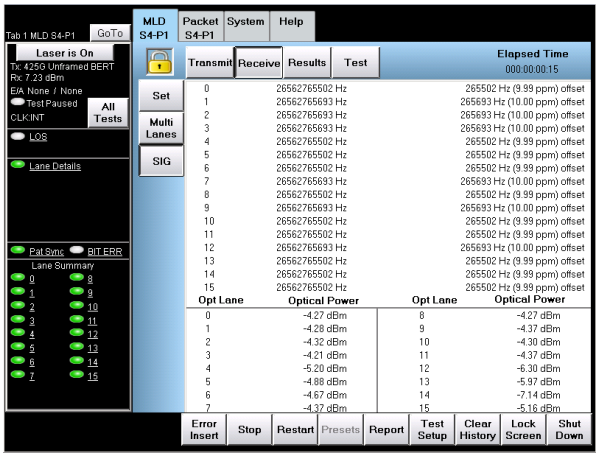
- Chassis Clock Sources, reference platform datasheet:
  - Internal stratum 3
  - 1.544 MHz, 2.048 MHz, BITS/1.544 Mbps, SETS/2.048 Mbps, 100/120 Ohm RJ-48
- Recovered: from the incoming signal
- External: 1.544 MHz, 2.048 MHz, 10 MHz, TTL level via 50 Ohm MMCX connector (connector shared with trigger input)

Line frequency Offset Generation

- Line frequency offset generation +/-300 ppm in 0.1 ppm steps, affects all lanes
- Constant generation
- Ramp generation: min offset, max offset, step size, and step duration settings

Line Frequency Measurement Capability

- Displays measured transmit line frequency offset in Hz
- Displays measured transmit line frequency offset from external reference clock in both Hz and ppm
- User defined alarm threshold for external transmit reference clock offset measurements
- Provides line frequency measurements in Hz with offset in Hz and ppm. Measures all lanes for Unframed BERT, single lane for 400GE
- User defined alarm threshold for received line frequency measurements



Reference Clock Outputs

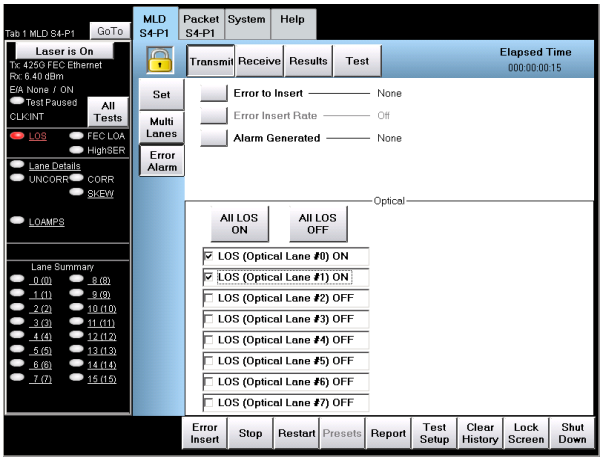
- Eye Clock out: 1/170th line rate, 50 Ohm MMCX connector (connector shared with trigger output)
- CFP8 module monitor clock output: 50 Ohm MMCX connector

Advanced Triggering

- Trigger in: TTL level via 50 Ohm MMCX connector (connector shared with external clock input)*
- Trigger out: TTL level via 50 Ohm MMCX connector (connector shared with eye clock out)*

CFP8 Optical Power Verification

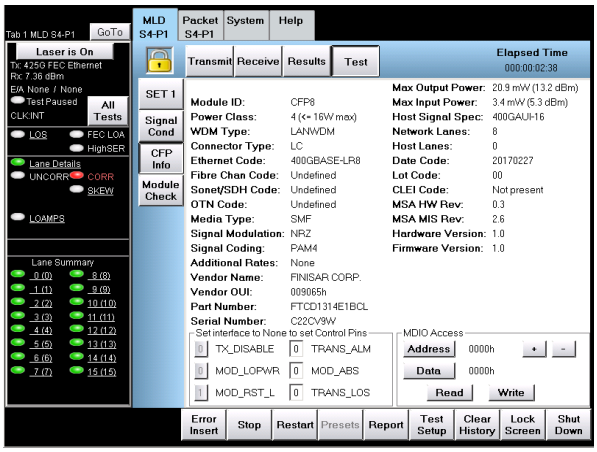
- Global and per optical lane power output enable/disable
- Received per lane and broadband optical power level monitoring
- User-defined alarm threshold for received optical power level



**For future application*

Transceiver CFP8 MDIO Testing

- Complete CFP8 MDIO access
- Raw read/write capability for all MDIO registers
- Formal display of commonly used fields
- Module hardware control pin read/write access



Transceiver Temperature Monitoring

- Measures current transceiver temperature in °C

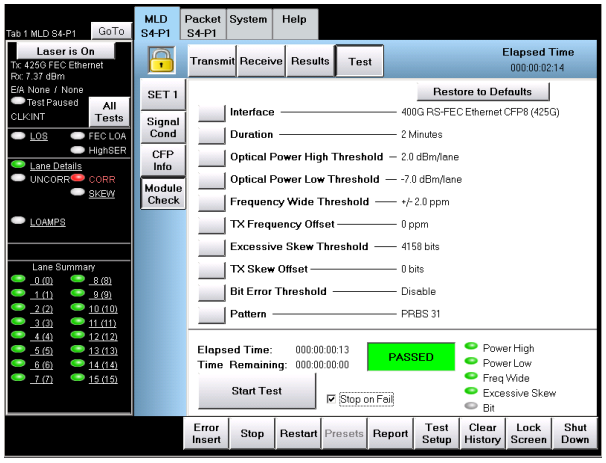
Transceiver 3.3V Power Testing

- Supports variable 3.3V input power to qualify transceiver specifications, up to +/- 5% adjustment in % or voltage (+/- 5%) to verity
- Measures the active 3.3V power
- Measures the active transceiver power consumption in watts

Transceiver Module Health Check

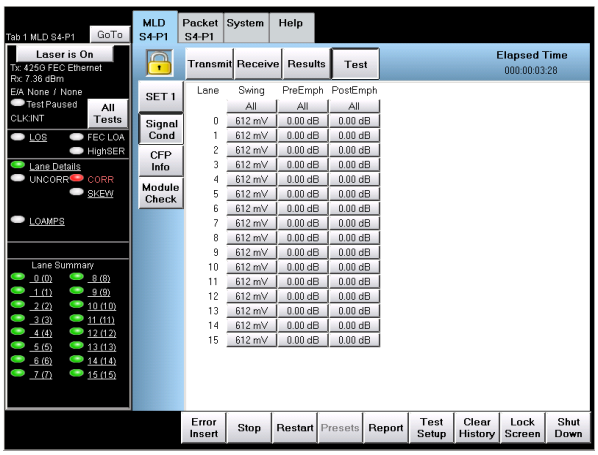
Simple one button pass/fail test for verifying all transceiver properties

- Advanced user defined thresholds
- Simple test report includes settings, results and CFP8 Module MDIO information



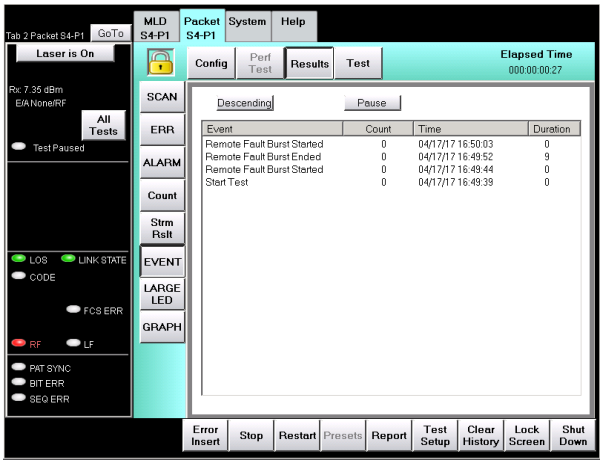
Advanced PHY Features

- Per lane user controllable swing, pre and post emphasis signal conditioning settings to stress transceiver interfaces
- TX Swing: 285 to 1087mV
- TX Pre Emphasis: 0.0 to 9.76dB
- TX Post Emphasis: 0.0 to 6.02dB
- Receiver auto-tune mode for best optimization of receive SerDes



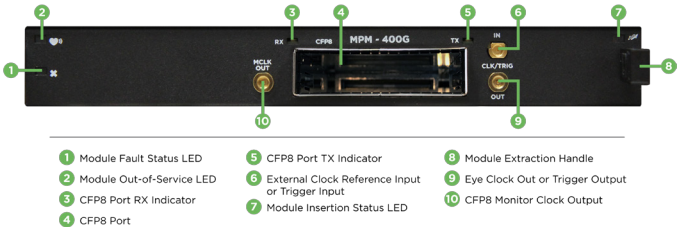
Results

- LEDs and detailed statistical counters
- Graphs and Histograms
- Event log history showing event, count, day/time, and duration for last 1,000 events
- Flexible test reporting options including PDF



Test Profiles

Supports save and restore of test profiles



General Specifications

- Double wide, single high test module
- Requires MPA chassis configured for double wide test modules

VeEX Inc.
2827 Lakeview Court
Fremont, CA 94538 USA
Tel: +1.510.651.0500
Fax: +1.510.651.0505
www.veexinc.com
customercare@veexinc.com

D05-00-131P B00 2019/3